

REMARKS:

Claims 1, 3, 4, 8, 9, and 13 have been amended and claims 15-21 added herein. Upon entry of this amendment, claims 1-13 and 15-21 will be pending in the above-identified Application.

Drawings

A marked copy of Figure 2 showing substitution of "E" for the second "D" in red is included for the Examiner's approval.

Claims 4-7 and 9 – Section 102 (Yamazaki)

Applicants respectfully request reconsideration of the rejection of claims 4-7 and 9 under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,246,070 (Yamazaki). As amended, claims 4-7 and 9 recite forming a gate electrode on a transparent substrate, and forming a gate insulating film on the gate electrode, wherein the gate insulating film comprises a silicon oxide film formed on a silicon nitride film.

Yamazaki discloses a semiconductor device having a substrate and a gate insulating film. Yamazaki does not disclose forming a gate electrode on a transparent substrate, or forming a gate insulating film on the gate electrode, wherein the gate insulating film comprises a silicon oxide film formed on a silicon nitride film.

Claim 9 further recites that subsequent to the dopant implanting step, defects formed in the protective insulating film are recovered by applying a temperature of about 600 degrees Centigrade. Though Yamazaki discloses an annealing technique for obtaining an activating effect of impurities (column 11, lines 28-32), it does not disclose that subsequent to a dopant implanting step, defects formed in the protective insulating film are recovered by applying a temperature of about 600 degrees Centigrade.

Because Yamazaki does not show every element of claims 4-7 and 9, the rejection is improper. Accordingly, Applicants request the rejection be withdrawn.

Claim 8 – Section 103 (Yamazaki in view of Ohtani)

Applicants respectfully request reconsideration of the rejection of claim 8 under 35 U.S.C. § 103(a) as being unpatentable over Yamazaki in view of U.S. Patent No. 6,063,654 (Ohtani). As amended, claim 8 recites that the protective insulating film is formed on a surface of the amorphous silicon film by surface oxidation of the amorphous silicon film, and then the amorphous silicon film is crystallized to form the polysilicon film, wherein the surface oxidation comprises exposing the amorphous silicon film to hot steam of about 400 degrees Centigrade.

Yamazaki discloses a semiconductor device comprising an insulating film and an amorphous silicon film. Ohtani discloses a method of manufacturing a TFT including formation of an oxide film. Yamazaki, Ohtani, and any combination of them fail to show or suggest surface oxidation comprising exposing the amorphous silicon film to hot steam of about 400 degrees Centigrade.

Because the prior art fails to show or suggest every element of claim 8, the rejection is improper. Accordingly, Applicants request the rejection be withdrawn.

Claim 11 – Section 103 (Yamazaki in view of Kawasaki)

Applicants respectfully request reconsideration of the rejection of claim 11 under 35 U.S.C. § 103(a) as being unpatentable over Yamazaki in view of U.S. Patent No. 6,281,552 (Kawasaki).

Because claim 11 includes the method of making a bottom-gate thin-film transistor recited in claim 4, the rejection of claim 11 is improper for the reasons stated above regarding claim 4. Accordingly, Applicants request the rejection be withdrawn.

Claim 13 – Section 103 (Yamazaki in view of Nakajima)

Applicants respectfully request reconsideration of the rejection of claim 13 under 35 U.S.C. § 103(a) as being unpatentable over Yamazaki in view of U.S. Patent No. 6,420,758 (Nakajima). As amended, claim 13 recites forming an organic EL element including a luminescent layer sandwiched between a first pair of layers

